IN THE CLAIMS

Please amend the claims as follows:

1. (original) Method of manufacturing a semiconductor device (10) with a field effect transistor, in which method a semiconductor body (1) of silicon is provided at a surface thereof with a source region (2) and a drain region (3) of a first conductivity type, which both are provided with extensions (2A,3A), and with a channel region (4) of a second conductivity type, opposite to the first conductivity type, between the source region (2) and the drain region (3) and with a gate region (5) separated from the surface of the semiconductor body (1) by a gate dielectric (6) above the channel region (4), and wherein a pocket region (7) of the second conductivity type and with a doping concentration higher than the doping concentration of the channel region (4) is formed below the extensions (2A,3A), and wherein the pocket region (7) is formed by implanting heavy ions in the semiconductor body (1), after which implantation a first annealing process is done at a moderate temperature and a second annealing process with a fast ramp-up is done at a higher temperature, characterized in that between the two annealing processes, amorphous silicon in the semiconductor body (1) is intentionally kept present in a surface region of the semiconductor body (1) which extends from the surface of the

semiconductor body up to about the projected range of the implanted pocket region (7).

2. (original) Method according to claim 1, characterized in that the first annealing process is stopped at the moment that re-growth of the semiconductor body (1), starting from the deepest border of a region comprising amorphous silicon, reaches about the projected range of the implanted pocket region (7).

3. (original) Method according to claim 1, characterized in that in the first annealing process all amorphous silicon in the semiconductor body (1) is removed and that an implantation of inert ions that re-introduces amorphous silicon into the semiconductor body (1), at least in a region around the projected range of the implanted pocket region (7), is applied between the first and the second annealing process.

4. (currently amended) Method according to claim 1~~, 2 or 3~~, characterized in that before the formation of the implanted pocket region (7), another implantation of inert ions is applied that introduces amorphous silicon into the semiconductor body at least in a region beyond the intended projected range of the implanted pocket region (7).

5. (currently amended) Method according to claim 3 ~~or 4~~, characterized in that for the implantation of inert ions, ions are chosen from a group comprising Ge, Si, Ar or Xe.

6. (currently amended) Method as claimed in ~~anyone of the preceding claims~~claim 1, characterized in that for the ions of the implanted pocket region (7) In ions are chosen.

7. (currently amended) Method as claimed in ~~anyone of the preceding claims~~claim 1, characterized in that the first annealing process is done at a temperature between 550 and 650 degrees Celsius and the second annealing process is done at a temperature higher than about 900 degrees Celsius.

8. (original) Method as claimed in claim 7, characterized in that the second annealing process is a rapid thermal annealing process to obtain flash or spike activation of the pocket region (7).

9. (currently amended) Method as claimed in ~~any one of the preceding claims~~claim 1, characterized in that the pocket region (7) and the extensions (2A,3A) of the source (2) and drain (3) are

formed at the same stage of the manufacturing of the semiconductor device (10).

10. (currently amended) A semiconductor device (10) comprising a field effect transistor obtained using a method as claimed in ~~any one of the preceding claims~~claim 1.